

8:00-8:45 **Continental Breakfast and Registration**

8:45-9:00 **Welcome and Introduction from General Co-Chair and Committee**

9:00-10:30 **Session I: System Vulnerability and Workload Effects**
Chair: Rakesh Kumar (UIUC)

The Effect of Input Data on Program Vulnerability.
Vilas Sridharan and David Kaeli.

Quantized AVF: A Means of Capturing Vulnerability Variations over Small Windows of Time.
Arijit Biswas, Niranjan Soundararajan, Shubhendu Mukherjee and Sudhanva Gurumurthi.

Soft Error Effect and Register Criticality Evaluations: Past, Present and Future.
Régis Leveugle, Laurence Pierre, Paolo Maistri and Renaud Clavel.

10:30-10:45 **Break**

10:45-12:15 **Session II: Applications / Case Studies**
Chair: Charles Recchia (Intel)

Evaluation of Low-Cost Detection and Recovery of Soft Errors in an ABS controller.
Daniel Skarin and Johan Karlsson

A Case Study of the Soft Errors Observed in I/O Adapters.
Anh Dang, Pia Sanda, Ricardo Mata and Subhasish Mitra.

Platform Neutron Testing for Single Event Upset (SEU).
Tsu-Yau Chuang, Eric Schmidt and Shi-Jie Wen.

12:15-12:45 **Lunch**

12:45-14:00 **Poster Session I**

Adapting to Intra-Die Variations in Transient Fault Susceptibilities.
Kenneth Zick and John Hayes

Testing the Critical Operating Point (COP) Hypothesis using FPGA Emulation of Timing Errors in Overscaled Soft-Processors. *Sriram Narayanan, Galen Lyle, Rakesh Kumar and Douglas L. Jones.*

Thermal Management in Reliably Overclocked Systems.
Prem Kumar Ramesh, Viswanathan Subramanian and Arun Somani.

Analysis of a Multiple Cell Upset Failure Model for Memories.
Sanghyeon Baeg, Pedro Reviriego, Juan Antonio Maestro, ShiJie Wen and Richard Wong.

Single-Threaded Mode AVF Prediction During Redundant Execution.
Blake C. Sutton and Sudhanva Gurumurthi.

Exploring the Synergy of Emerging Workloads and Silicon Reliability Trends.
Marc de Kruijf and Karu Sankaralingam.

14:00-14:15 **Break**

14:15-16:15 **Session III: SER Measurement and Modeling**
Chair: Steve Walstra (Intel)

Neutron Beam Irradiation Study of Workload Dependence of SER in a Microprocessor.
Ted Hong, Sarah Michalak, Todd Graves, Jerry Ackaret, Sonny Rao, and Subhasish Mitra.

Trends from Ten Years of Soft Error Experimentation.
Anand Dixit, Raymond Heald and Alan Wood.

Comparison of Alpha-particle and Neutron-induced Combinational and Sequential Logic Error Rates at the 32nm Technology Node.
Balkaran Gill, Norbert Seifert and Victor Zia.

Soft-Error Cross-Section Mapping and Rate Prediction using Accurate Simulation.
Klas Lilja.

16:15-16:30 **Break**

16:30-17:15 **Panel: “System Specifications of Soft Error Performance”**

Moderator: Adrian Evans (Cisco)

Panelists: Pia Sanda (IBM)
Allan Silburt (Cisco)
Yaakov Kogan (AT&T)
Sarah Michalek (LANL)

17:15-18:00 **Birds of a Feather Sessions**

Moderator: Jeff Wilkinson (Medtronic)

Birds of a Feather sessions provide small groups the opportunity to gather for a short discussion and planning meeting related to a specific topic. Three rooms have been reserved for these short sessions. One session has been planned and the others will be announced by lunchtime of day 1. E-mail suggestions to publications@selse.org or speak to one of the workshop organizers onsite.

Session A: Embedded systems derating:

How many soft errors lead to system failure in a small system?

Moderator: Jeff Wilkinson (Medtronic)

Studies have been published describing the derating values to use to predict the fraction of soft-errors that lead to system errors. Most of these studies have concentrated on this question using large scale computer systems that are highly optimized for soft-error tolerance. Two recent papers on embedded system derating suggest that the values are quite different for simpler microprocessor architectures.

Participants will be asked to consider:

- Is there a real difference between these classes of systems?*
- How should derating be defined for embedded systems?*
- What projects or avenues of research are likely to be profitable to further investigation of this topic?*

Session B and C: TBD

18:00- **Dinner and Reception**

7:45-8:30 **Continental Breakfast**

8:30-9:15 **Report From Birds of Feather Sessions**

9:15-10:15 **Session IV: Mitigation Techniques – Logic**
Chair: Charles Slayman (Sun)

A Coarse-Grained Dynamically Reconfigurable Architecture Enabling Flexible Reliability.
Dawood Alnajjar, Younghun Ko, Takashi Imagawa, Masayuki Hiromoto, Yukio Mitsuyama, Masanori Hashimoto, Hiroyuki Ochi and Takao Onoye.

Fault-Tolerant Resynthesis for Dual-Output LUTs.
Ju-Yueh Lee, Yu Hu, Rupak Majumdar, Lei He and Minming Li.

10:15-10:30 **Break**

10:30-12:00 **Session V: Microprocessors**
Chair: Jim Tschanz (Intel)

A Low-Overhead Technique to Protect the Issue Control Logic Against Soft Errors.
Javier Carretero, Xavier Vera, Jaume Abella, Pedro Chaparro and Antonio González

Voltage Noise: Why It's Bad, and What To Do About It. *Vijay Janapa Reddi, Meeta S. Gupta, Krishna K. Rangan, Glenn Holloway, Gu-Yeon Wei, Michael D. Smith and David Brooks*

A Detector for Harmful Errors.
Jing Yu and Maria Garzarán

12:00-12:45 **Lunch**

12:45-14:00 **Poster Session II**

NBTI-Aware Dynamic Instruction Scheduling.
Taniya Siddiqua and Sudhanva Gurumurthi.

Implementation and Validation of a Low-Cost Single-Event Latchup Mitigation Scheme.
Michael Nicolaidis, Kholdoun Torki, Federico Natali, Kader Belhaddad and Dan Alexandrescu.

A Foundation for the Accurate Prediction of the Soft Error Vulnerability of Scientific Applications.
Greg Bronevetsky, Bronis R. de Supinski and Martin Schulz.

Soft-error Mitigation at the Architecture-Level Using Berger Codes and Instruction Repetition.
Daniel Limbrick, Edward Ossi, Bharat Bhuva and William Robinson.

3D Simulation and Analysis of the Radiation Tolerance of Voltage Scaled Digital Circuits.
Rajesh Garg and Sunil Khatri.

14:00-14:45 **Invited Talk: Helmet Puchner, Cypress Semiconductor**
“On The Accuracy of Accelerated and Life Soft Error Testing”

14:45-15:00 **Break**

15:00-16:30 **Session VI: Mitigation Techniques – Arrays and Sequentials**
Chair: Terry Garyet (Freescale)

Soft Error Mitigation Schemes for High Performance and Aggressive Designs.
Naga Durga Prasad Avirneni, Viswanathan Subramanian and Arun Somani.

Protecting Prediction Arrays against Faults.
Yiannakis Sazeides, Costas Kourouyiannis, Nikolas Ladas and Veerle Desmet.

Modeling SRAM Failure Rates to Enable Fast, Dense, Low-Power Caches.
Jangwoo Kim, Mark McCartney, Ken Mai and Babak Falsafi.

16:30-17:00 **Closing Discussion**