SELSE 6
Day 1 – March 23rd, 2010
Stanford University

8:00-8:45 **Continental Breakfast and Registration**

8:45-9:00 **Welcome and Introduction from General Co-Chair and Committee**

9:00-10:15 **Session I: High Performance Computing**
Chair: Charles Recchia (Intel)

Invited Talk : High Performance Computing Requirements
John Daly (Center for Exceptional Computing).

Statistical Fault Detection for Parallel Applications with AutomaDeD.
Greg Bronevetsky, Ignacio Laguna, Saurabh Bagchi, Bronis R. de Supinski, Martin Schulz and Dong Ahn.

10:15-10:30 **Break**

10:30-12:15 **Session II: Modeling SER**
Chair: TBD

Invited Talk : CMOS Process Variations – Critical Operating Point Hypothesis.
Janak Patel (University of Illinois).

Using PVF Traces to Accelerate AVF Modeling.
Vilas Sridharan and David Kaeli.

Formal Diagnosis of Hardware Transient Errors in Programs.
Layali Rashid, Karthik Pattabiraman and Sathish Gopalakrishnan.

12:15-13:15 **Lunch**

13:15-15:00 **Session III: SER Measurement 1**
Chair: TBD

Invited Talk : Measurement Techniques.
Steve Wender, (Los Alamos National Laboratories).

Accuracy of Various Broad Spectrum Neutron Sources for Accelerated Soft Error Testing.
Charles Slayman.

The Impact of New Technology on Soft Error Rates.
Anand Dixit, Raymond Heald and Alan Wood.

15:00-15:15 **Break**

15:15-16:45 **Session IV: SER Measurement 2**
Chair: TBD

Neutron Soft Error Rate Testing of AMD Microprocessors.
Seth Prejean.

Measurement Results of Multiple Cell Upsets on a 65nm Tapless Flip-Flop Array.
Jun Furuta, Kazutoshi Kobayashi and Hidetoshi Onodera.

A Multi-Partner Soft Error Rate Analysis of an InfiniBand Host Channel Adapter.
Hillel Chapman, Evelyn Landman, Ayelet Margalit-Ilovich, Yi-Pin Fang, Anthony S. Oates, Dan Alexandrescu and Olivier Lauzeral.

16:45-17:00 **Break**

17:00-18:00 **Panel**: Relating Measured Soft Error Measurements to Predicted Behaviours

18:00 **Reception and Dinner**

8:00-8:30 **Continental Breakfast**

8:30-10:45 **Session V: Circuit Level Modeling and Measurement**
Chair: TBD

Invited Talk : Modeling and Analysis of SER In Combinatorial Circuits.
Natasa Miskov-Zivanov, Carnegie Mellon Unversity.

Design of a Sequential Logic Cell Using LEAP: Layout Design Through Error Aware Placement.
Hsiao-Heng Lee, Klas Lilja and Subhasish Mitra.

On the Radiation-Induced Soft Error Performance of Hardened Sequential Elements in Advanced Bulk CMOS Technologies.
Norbert Seifert, Vinod Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, and A. Balasubramanian.

10:45-11:00 **Break**

11:00-12:00 **Session VI: Microprocessors III**
Chair: TBD

Logic Soft Errors in a Parallel CISC Decoder.
Eric Hill and Mikko Lipasti.

Exploiting Short-Lived Values for Performance-Reliability Trade-off in Soft-Error Tolerant Superscalar Data Paths.
Ehab Ababneh.

12:00-13:00 **Lunch**

13:00-14:00 **Poster Session**

Resil: A Resiliency Hardware/Software Framework for ASIPs.
Tuo Li, Roshan Ragel and Sri Parameswaran.

Concurrent Autonomous Self-Test for Uncore Components in SoCs.
Yanjing Li, Donald Gardner and Subhasish Mitra.

Reliability-Aware Synthesis: XOR Logic Function Case Study.
Daniel Limbrick, William Robinson and Bharat Bhuva.

The Effect of Pipeline Depth on Logic Soft Errors.
Eric Hill and Mikko Lipasti.

A Bulk Current Sensor to Detect Single-Event Transients
Tao Wang, Zhichao Zhang, Li Chen, Anh Dinh, and Robert Shuler.

14:00-14:15 **Break**

14:15-15:15 **Session VII: Mitigation Techniques**
Chair: TBD

A Numerical Optimization-based Methodology for Application Robustification.
Joseph Sloan, David Kesler, Rakesh Kumar and Ali Rahimi.

On-Line Detection and Correction of Errors Due to Fast, Dynamic Voltage Droop Events.
Jim Tschanz and Keith Bowman.

15:15-16:00 **Session VIII: Cross Layer Reliability**

Invited Talk : Cross-Layer Reliability.
Nick Carter (Intel).

16:00-16:30 Discussion: Cross-Layer Reliability.

16:30-17:00 **Closing Remarks**